SIDDAGANGA INSTITUTE OF TECHNOLOGY, TUMAKURU

LECTURE PLAN FOR THE ACADEMIC YEAR 2025 – 2026

Teacher	Dr.M S RUDRAMURTHY	**Dept.**	Information Science & Engineering
Class	III Semester, E Section	**Course**	**Integrated Course:** S3ISI01: Digital Circuits & Computer Organization
Contact Hours/Week	3L+0T (Credits: 4.0)		CIE Marks: 50 SEE Marks: 50

Course Learning objectives:

This course will enable students to:

1.	**Learn the different techniques of simplification of Boolean expressions and design of combinational circuits.**
2.	**Design of counters and registers for the real time applications.**
3.	**Understand the fundamental concepts of computer organization and gain insight into the addressing modes and execution of an instruction in a single bus CPU.**
4.	**Apply the different computer arithmetic techniques to solve the problems.**

Course Code	**Course Title**	**Teaching & Learning Scheme**							
		Classroom Instruction (CI) (in hrs / sem)		**Lab Instruction (LI) (in hrs / sem)**	**Self-Learning (SL) (in hrs / sem)**	**Term Work (TW) (in hrs / sem)**	**Assessment (hrs / sem)**	**Total no. of Hours per sem**	**Total Credits (C)* (Total Hours/30)**
		L	**T**	**P**	**SL**	**TW**	**A**		
S3ISI01	Digital Circuits & Computer Organization	**42**	**-**	**26**	**15**	**30**	**07**	**120**	**4**

SL. No.	**DATE**	**TOPIC**	**REMARKS**
		UNIT – I	
1	01-09-2025	Introduction to Digital System: Boolean Algebra and Boolean Functions,	
2	03-09-2025	min-term and max-term notations. Simplification of Boolean expressions using Boolean laws and Rules,	
3	04-09-2025	Simplification of Boolean expressions using Boolean laws and Rules,	
4	08-09-2025	Simplification of Boolean expressions using Karnaugh map techniques.	
5	10-09-2025	Simplification of Boolean expressions using Karnaugh map techniques	
6	11-09-2025	Simplification of Boolean expressions using Karnaugh map techniques	
7	12-09-2025	Design of combinational Logic Circuits:	
8	15-09-2025	Design of Decoders,	
9	17-09-2025	Multiplexers, Demultiplexers.	Assignment 1
10	18-09-2025	Self-Study Hours: Problems and solutions	
11	19-09-2025	Selft Study Hours: Problems and solutions	

		UNIT-II	
12	22-09-2025	Sequential Logic Circuits: Flip Flops: Introduction to Flip-Flops,	
13	24-09-2025	Types of Flip-Flops: RS FF, SR FF,	
14	25-09-2025	JK FF and M/S JK FF.	
15	29-09-2025	Counters: Definition of Counter, Types of Counters, Design of Asynchronous Counters.	
16	03-10-2025	Registers: Basic Register, Shift-Register, Types of Shift Registers,	
17	06-10-2025	Unidirectional and Bidirectional Shift Register,	
18	08-10-2025	Johnson counter and Ring Counters.	Assignment 2
19	09-10-2025	Selft Study Hours: Problems and solutions	
20	10-10-2025	Selft Study Hours: Problems and solutions	
		UNIT-III	
21	13-10-2025	Basic Structure of Computer: Functional Units,	
22	15-10-2025	Basic Operational Concepts, Bus Structures,	
23	16-10-2025	Performance - Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement.	
24	17-10-2025	Machine Instructions and Programs: Numbers, Arithmetic Operations and	
25	20-10-2025	Characters - Number Representation,	
26	22-10-2025	Addition of Positive Numbers,	
27	23-10-2025	Addition and Subtraction of Signed Numbers,	
28	24-10-2025	Overflow in Integer Arithmetic,	
29	29-10-2025	Characters, Memory Location and Addresses - Byte Addressability	Assignment 3
30	30-10-2025	Selft Study Hours: Problems and solutions	
31	31-10-2025	Selft Study Hours: Problems and solutions	
		UNIT-IV	
32	03-11-2025	Addressing modes-Implementation of Variables and Constants,	
33	10-11-2025	Indirection and Pointers, Indexing and Arrays, Relative Addressing, Additional Modes.	
34	12-11-2025	Basic Processing Unit: Execution of a Complete Instruction	
35	13-11-2025	Branch Instructions, Multiple Bus Organization,	
36	14-11-2025	Design of Asynchronous Up and Down Counters.	
37	17-11-2025	Hard wired Control - A Complete Processor,	
38	19-11-2025	Micro programmed Control -Microinstructions.	Assignment 4
39	20-11-2025	Selft Study Hours: Problems and solutions	
40	21-11-2025	Selft Study Hours: Problems and solutions	
		UNIT-V	
41	24-11-2025	Arithmetic: Addition and Subtraction of Signed Numbers - Addition/Subtraction Logic Unit,	
42	26-11-2025	Multiplication of Positive Numbers,	
43	27-11-2025	Signed Operand Multiplication - Booth Algorithm,	
44	28-11-2025	Fast Multiplication - Bit-Pair Recoding of Multipliers,	Assignment 5
45	01-12-2025	Carry-Save Addition of Summands, Integer Division,	
46	03-12-2025	Floating-point Numbers and Operations - IEEE Standard for Floating-Point Numbers,	
47	04-12-2025	Arithmetic Operations on Floating-Point Numbers - Addition and Subtraction Operations	
48	05-12-2025	Arithmetic Operations on Floating-Point Numbers - Addition and Subtraction Operations	
49	08-12-2025	Arithmetic Operations on Floating-Point Numbers - Addition and Subtraction Operations	
50	10-12-2025	Selft Study Hours: Problems and solutions	
51	11-12-2025	Selft Study Hours: Problems and solutions	

TEXT BOOKS:

1.	**Thomas L Floyd, Digital Fundamentals**	**Digital Fundamentals, Pearson Publications. Ed.11, 2020.**
2.	**Carl Hamacher, Zvonko Vranesic, SafwatZaky**	**Computer Organization, Tata McGraw Hill, ED.5, 2017**

REFERENCE BOOKS:

1.	**Donald P Leach, Albert Paul Malvino and Goutam Saha**	**Digital Principles and Applications, Tata McGraw – Hill, Ed.8, 2014**
2.	**Ronald J Tocci, Neil S Widmer, Gegory L. Moss.**	**Digital Systems-Principles and Applications, Pearson Education, Ed.12. 2016.**

LABORATORY PROGRAMS LIST:

Sl.No	Dates	Experiment
1	**01-09-2025, 04-09-2025 and 12-09-2025**	**Introduction to Electronics: Truth Table Verification of Basic Logic Gates.**
2	**08-09-2025, 11-09-2025 and 19-09-2025**	**Design and implementation of Half-adder and Full adder using minimum number of NAND gates only.**
3	**22-09-2025, 05-09-2025 and 26-09-2025**	**Design and implement a 3-variable SOP expression using a dual 4:1 MUX IC74LS153.**
4	**29-09-2025, 06-10-2025 and 10-10-2025**	**Design and implement the Full adder and Full subtractor using decoder and other logic gates.**
5	**09-10-2025, 13-10-2025 and 17-10-2025**	**Implement the following using 4-bit shift register IC 74LS95. a) Right Shift b) SISO c) PIPO d) PISO e) SIPO f) Left Shift g) Ring Counter h) Johnson Counter.**
6	**20-10-2025, 23-10-2025 and 24-10-2025**	**Test 1**
7	**27-10-2025, 30-10-2025 and 31-10-2025**	**Design a sequence generator to generate the given sequence using shift Register IC and other gates.**
8	**03-11-2025, 06-11-2025 and 07-11-2025**	**Design and implement 3-stage Asynchronous (mod-8) counter using MS J-K flip flops IC7476.**
9	**10-11-2025, 13-11-2025 and 14-11-2025**	**Implement UP-Down pre-settable counter using IC 74LS190 for the given mod N.**
10	**17-11-2025, 20-11-2025 and 21-11-2025**	**Design and implementation of Three-bit Synchronous Counter.**
11	**24-11-2025, 27-11-2025 and 28-11-2025**	**Test 2**
12	**01-12-2025, 05-12-2025 and 06-12-2025**	**Repetition classes**
	08-12-2025, 11-12-2025 and 12-12-2025	**Repetition classes**

Course Outcomes:

After the completion of this course, students will be able to:

CO1: **Design** combinational logic circuits for the required applications**. [L4]**
CO2: **Design** sequential logic circuits such as counters and registers for the specific needs**. [L4]**
CO3: **Analyze** the performance of a basic computer system. **[L3]**
CO4: **Design** control sequence for the given instruction on different CPU bus structures. **[L4]**
CO5: **Apply** appropriate technique to solve arithmetic related problems in computer. **[L4]**

Mapping of Course Outcomes (COs) to Program Outcomes (POs) & Program Specific Outcomes (PSOs):

		POs												PSOs		
		1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
COs	CO1	2	2												2	
	CO2	2	2	2											2	
	CO3	2	2	1											2	
	CO4	2	2	1											2	
	CO5	2	1	1											2	
	AVG	2	2	2											2	

Assessment Tools	COs				
Direct AT	**CO1**	**CO2**	**CO3**	**CO4**	**CO5**
CIE (Individual)	√	√	√	√	√
SEE (Individual)	√	√	√	√	√
Assignments (Individual/Group)	√	√	√	√	√
Micro Projects (Group)	-	-	-	-	-
Topic seminar (Individual)	-	-	-	-	-
Case studies (Individual/Group)	-	-	-	-	-
Online courses (Individual)	-	-	-	-	-
Indirect AT	**CO1**	**CO2**	**CO3**	**CO4**	**CO5**
Course end survey (Students)	√	√	√	√	√
Student profile (Faculty)	-	-	-	-	-

Course delivery methods, assessment tools and sample questions:

CO1	**Design** combinational logic circuits for the required applications
Delivery Methods	Chalk and talk, PPT
Assessment Tools	CIE, SEE, Assignment
Sample Questions	Q1. Design a 3-to-8-line Decoder and show how it can be used to realize a Full adder. (L3) Q2. Design a 8:1 Multiplexer and show how it can be used to realize a Full adder. (L3)

CO2	**Design** sequential logic circuits such as counters and registers for the specific needs**.**
Delivery Methods	Chalk and talk, PPT
Assessment Tools	CIE, SEE, Assignment
Sample Question	Q1. Show how a T-FF can be used as a frequency divider. (L3) Q2. Design a three-bit asynchronous UP and Down Counter using only M/S JK Flip Flops. Also, draw its timing diagram which illustrates the operation of the counter. (L3)

CO3	**Analyze** the performance of a basic computer system.
Delivery Methods	Chalk and talk, PPT
Assessment Tools	CIE, SEE, Assignment
Sample Question	Q1. The effective value of S for a RISC machine is 1.2 and for CISC, it is 1.5 both machines have the same clock rate R. The time for execution on the CISC machine is to be less than that of RISC machine. For this to happen, what is the largest allowable value for N, the number of instructions executed on the CISC machine, expressed as a percentage of the N value for the RISC machine. (L3) Q2. Explain the different basic instruction types. Show how the operation R=(A*B) -(C/D) can be implemented using any two instruction types. (L3)

CO4	**Design** control sequence for the given instruction on different CPU bus structures.
Delivery Methods	Chalk and talk, PPT
Assessment Tools	CIE, SEE, Assignment
Sample Question	Q1. Distinguish between Hardwired Controller and Microprogrammed Controller. (L2) Q2. Write the control signal sequence required to execute the instruction MOVE R2, (R1) in a Single bus CPU Organization. (L3)

CO5	**Apply** appropriate technique to solve arithmetic related problems in computer.
Delivery Methods	**Chalk &Talk/PPT**
Assessment Tools	Quiz, Test and Assignment
Sample Questions	Q1. Explain briefly the working principle of a Booth multiplier with an example. Give the flow chart for the Booth multiplication. (L3) 2. Multiply 13 and -6 using Bit-Pair Recoding of Multiplier method. (L3)

Sl No	Important Events	Date
1	Commencement of classes	01-09-2025
2	I – Test	13th -15th October 2025
3	Last date for dropping of course	21st October 2025
4	II – Test	27th -29th November 2025
5	Last date for withdrawal of course	01st December 2025
6	Last working day	13th December 2025
7	Preparation Holidays	14th Dec to 19th Dec2025
8	Semester end examination	20th Dec 2025 to 05-012026
9	Announcement of results	17th January 2026

Activities to meet Teaching Learning Scheme

Sl No	Activity Planned	Number of Hours
1.	Class Room Teaching	**42**
2.	Practical Hours	**26**
3	Self-Learning Hours	**15**
4.	Formative Assessment [Test (2 No.) +Quiz (2 No.) + Semester End Exam]	**07**
5.	**Activity Based Learning:** **I. Case Study (15 Hours) – (i) Design the solution for the given problem.** a. Understanding the Problem b. Design the solution c. Analysis and Conclusion **II. Case Study (15 Hours)** (ii) **Design the solution for the given problem.** 1. Understand the problem 2. Design the solution 3. Implement the solution	**30**
	Total Hours	**120**

Teacher

HOD 02/9/25

Principal 2/9/2025